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PATENT & TRADEMARK OFFICE

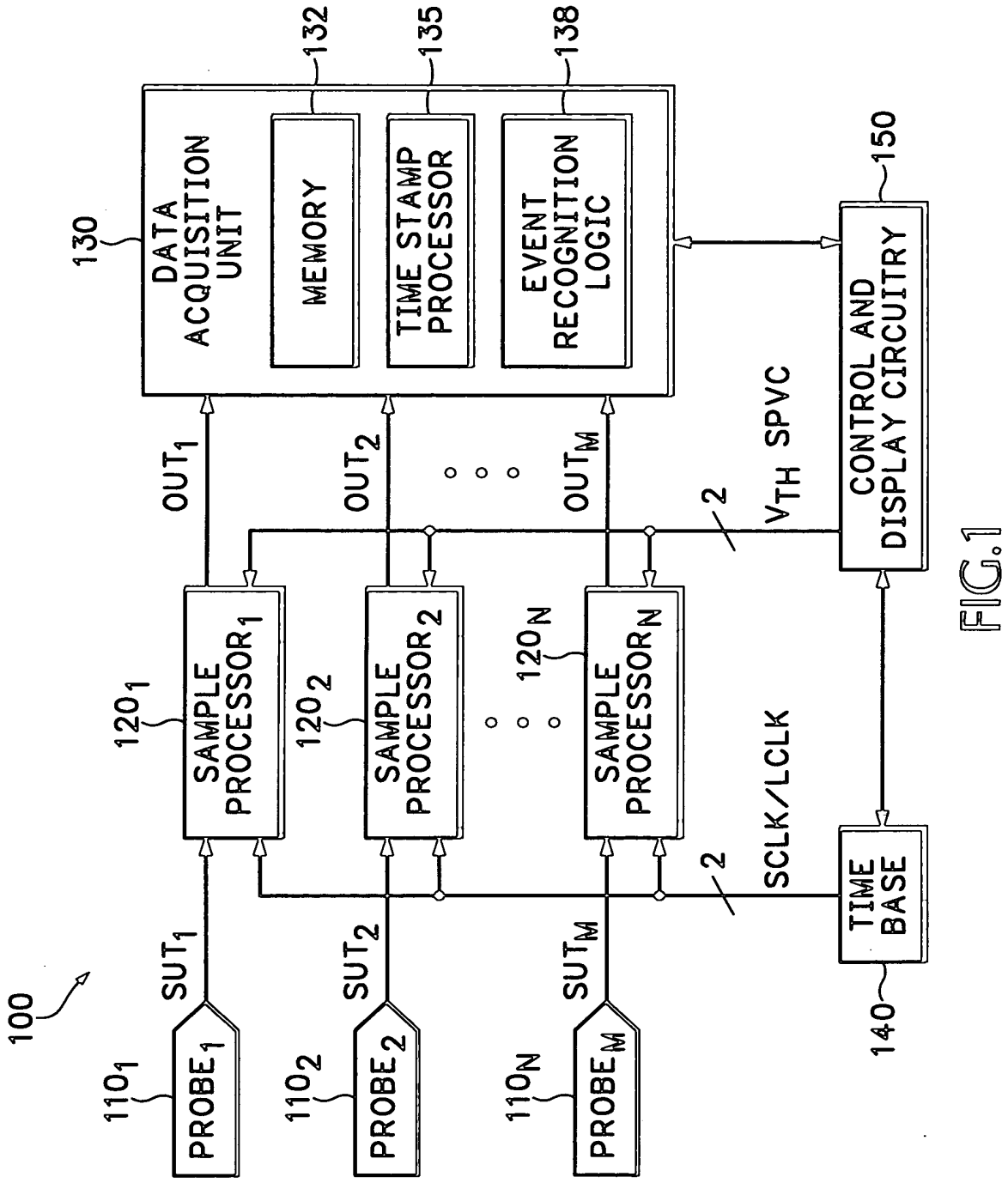

FIG.1

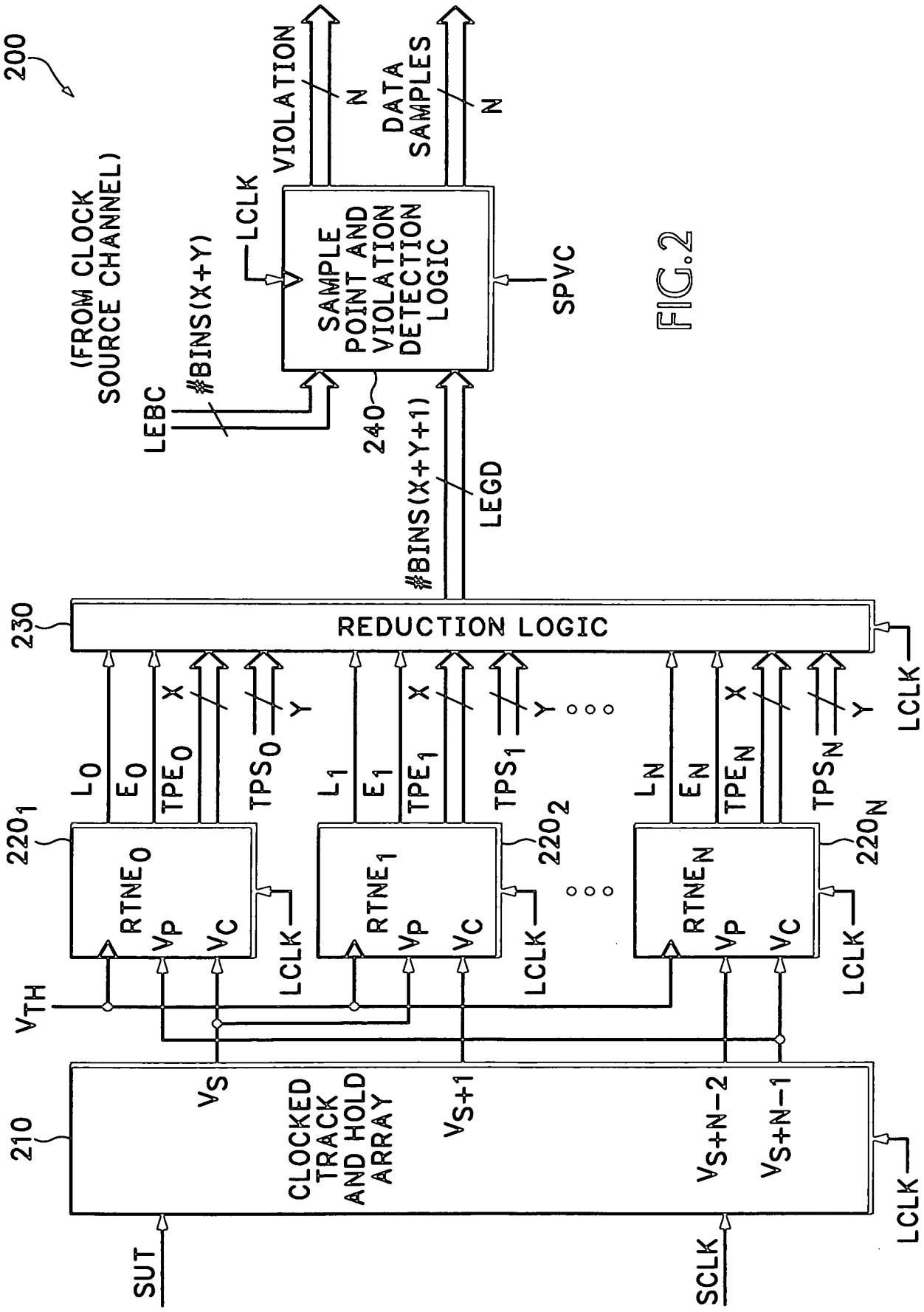
200
(FROM CLOCK SOURCE CHANNEL)
LEBC
#BINS(X+Y)
LCLK
SAMPLE POINT AND VIOLATION DETECTION LOGIC
240
VIOLATION
N
DATA SAMPLES
N
SPVC
#BINS(X+Y+1)
LEGD
230
REDUCTION LOGIC
LCLK
L_0
E_0
TPE_0
X
TPS_0
Y
L_1
E_1
TPE_1
TPS_1
L_N
E_N
TPE_N
TPS_N
220_1
220_2
220_N
$RTNE_0$
$RTNE_1$
$RTNE_N$
V_P
V_C
V_{TH}
210
CLOCKED TRACK AND HOLD ARRAY
V_S
V_{S+1}
V_{S+N-2}
V_{S+N-1}
SUT
SCLK

FIG.2

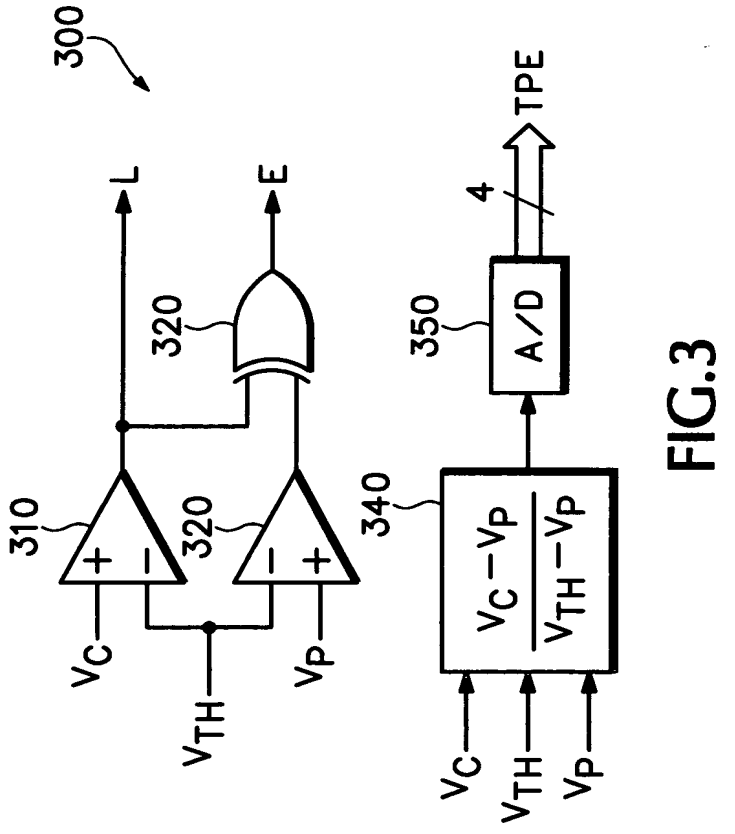

FIG.3

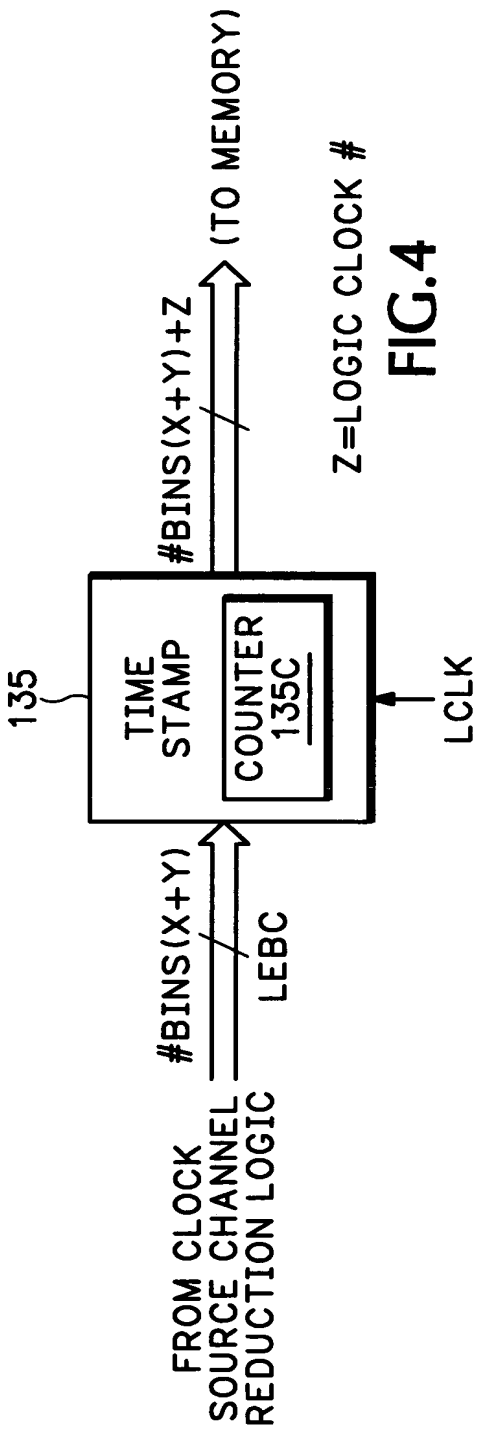
FROM CLOCK SOURCE CHANNEL REDUCTION LOGIC
#BINS(X+Y)
LEBC
135
TIME STAMP
COUNTER 135C
LCLK
#BINS(X+Y)+Z
(TO MEMORY)
Z=LOGIC CLOCK #

FIG.4

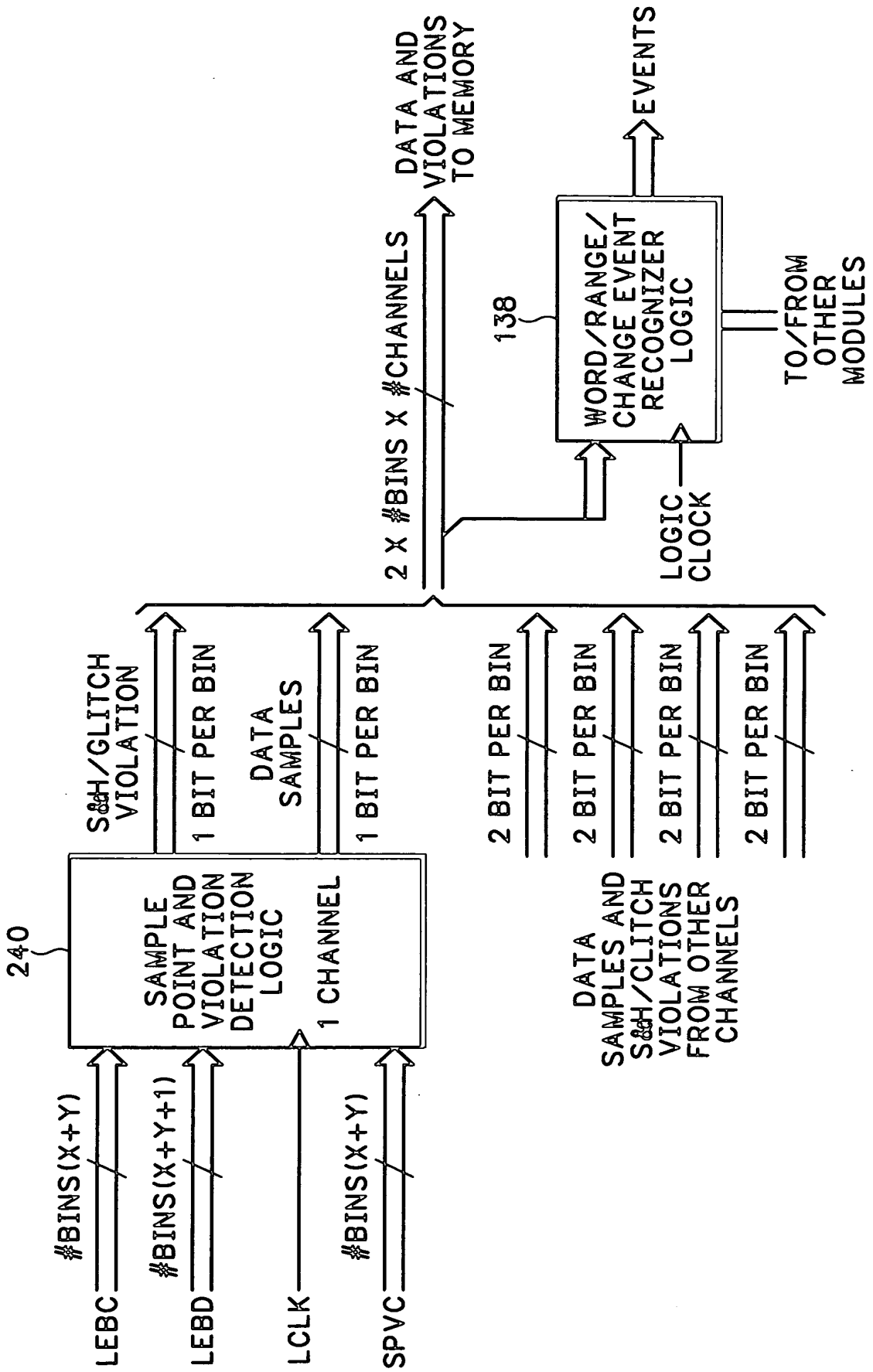
LEBC
#BINS(X+Y)
LEBD
#BINS(X+Y+1)
LCLK
SPVC
#BINS(X+Y)
240
SAMPLE POINT AND VIOLATION DETECTION LOGIC
1 CHANNEL
S&H/GLITCH VIOLATION
1 BIT PER BIN
DATA SAMPLES
1 BIT PER BIN
DATA SAMPLES AND S&H/CLITCH VIOLATIONS FROM OTHER CHANNELS
2 BIT PER BIN
2 BIT PER BIN
2 BIT PER BIN
2 BIT PER BIN
2 X #BINS X #CHANNELS
DATA AND VIOLATIONS TO MEMORY
138
WORD/RANGE/ CHANGE EVENT RECOGNIZER LOGIC
LOGIC CLOCK
EVENTS
TO/FROM OTHER MODULES

FIG.5

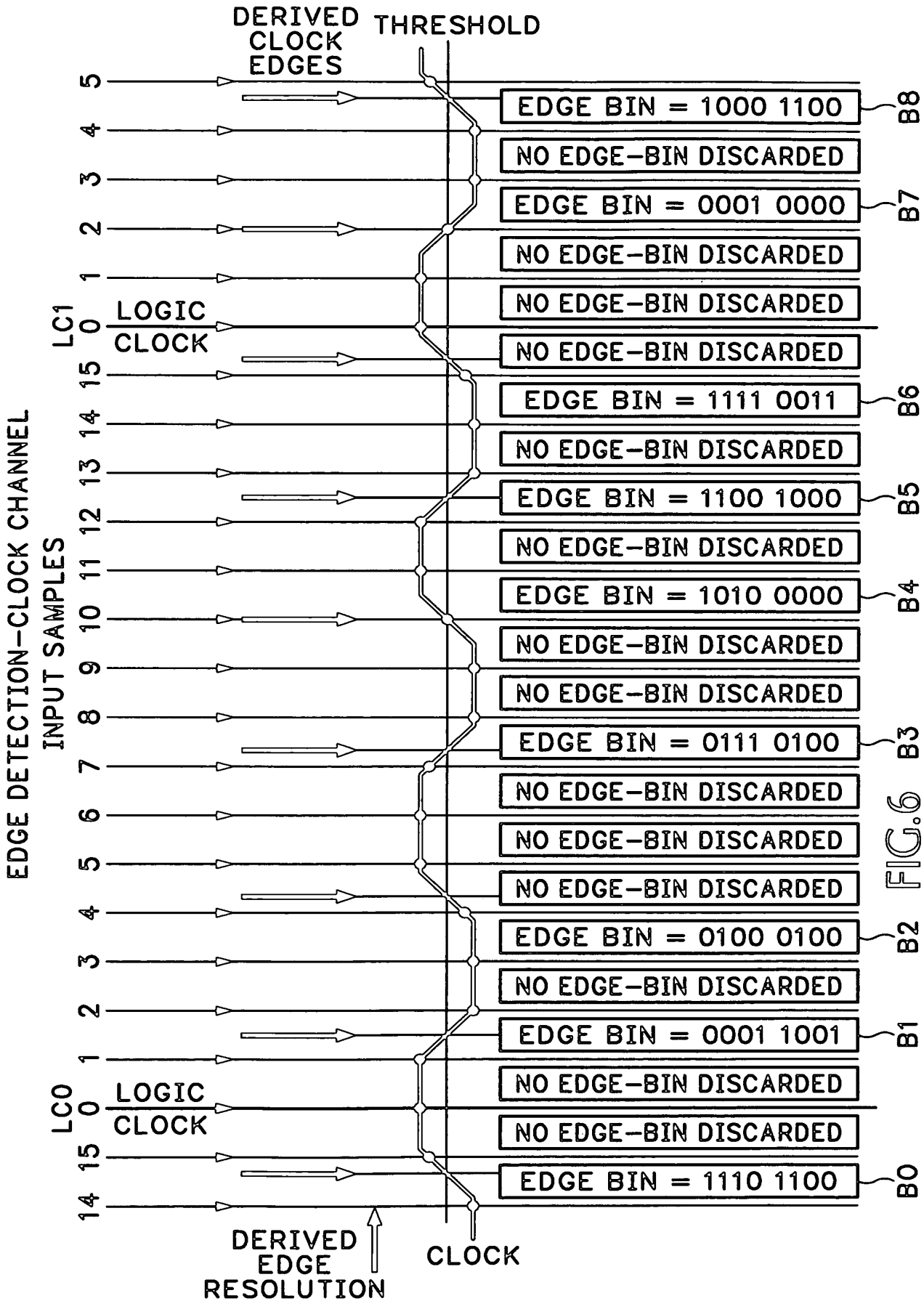
DERIVED CLOCK EDGES
THRESHOLD
EDGE DETECTION-CLOCK CHANNEL INPUT SAMPLES
LC1
LOGIC CLOCK
LC0
LOGIC CLOCK
EDGE BIN = 1000 1100
B8
NO EDGE-BIN DISCARDED
EDGE BIN = 0001 0000
B7
NO EDGE-BIN DISCARDED
NO EDGE-BIN DISCARDED
NO EDGE-BIN DISCARDED
EDGE BIN = 1111 0011
B6
NO EDGE-BIN DISCARDED
EDGE BIN = 1100 1000
B5
NO EDGE-BIN DISCARDED
EDGE BIN = 1010 0000
B4
NO EDGE-BIN DISCARDED
NO EDGE-BIN DISCARDED
EDGE BIN = 0111 0100
B3
NO EDGE-BIN DISCARDED
NO EDGE-BIN DISCARDED
NO EDGE-BIN DISCARDED
EDGE BIN = 0100 0100
B2
NO EDGE-BIN DISCARDED
EDGE BIN = 0001 1001
B1
NO EDGE-BIN DISCARDED
NO EDGE-BIN DISCARDED
EDGE BIN = 1110 1100
B0
DERIVED EDGE RESOLUTION
CLOCK

FIG.6

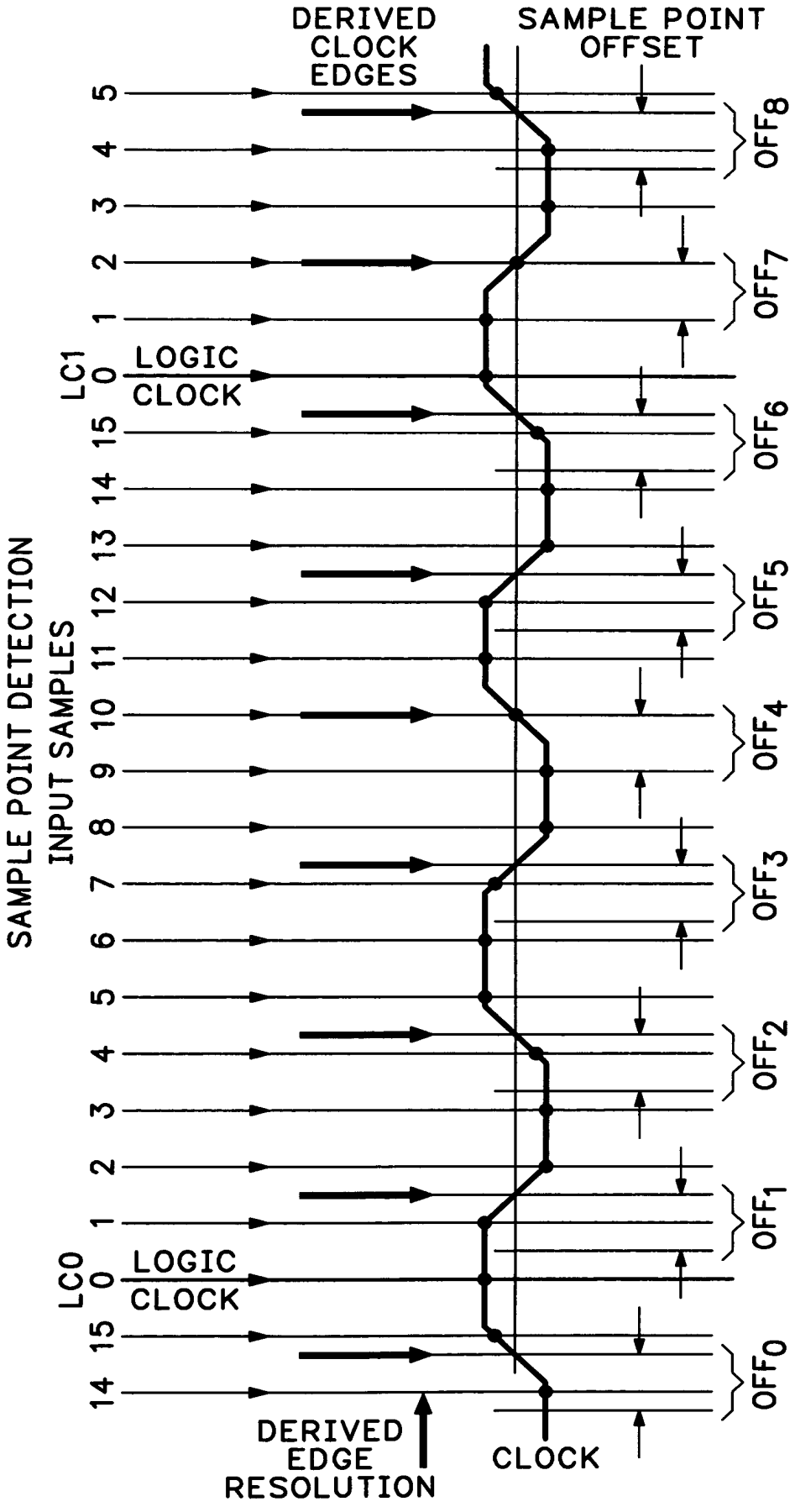
DERIVED CLOCK EDGES
SAMPLE POINT OFFSET
SAMPLE POINT DETECTION INPUT SAMPLES
LC1
LOGIC CLOCK
LC0
LOGIC CLOCK
OFF8
OFF7
OFF6
OFF5
OFF4
OFF3
OFF2
OFF1
OFF0
DERIVED EDGE RESOLUTION
CLOCK

FIG.7

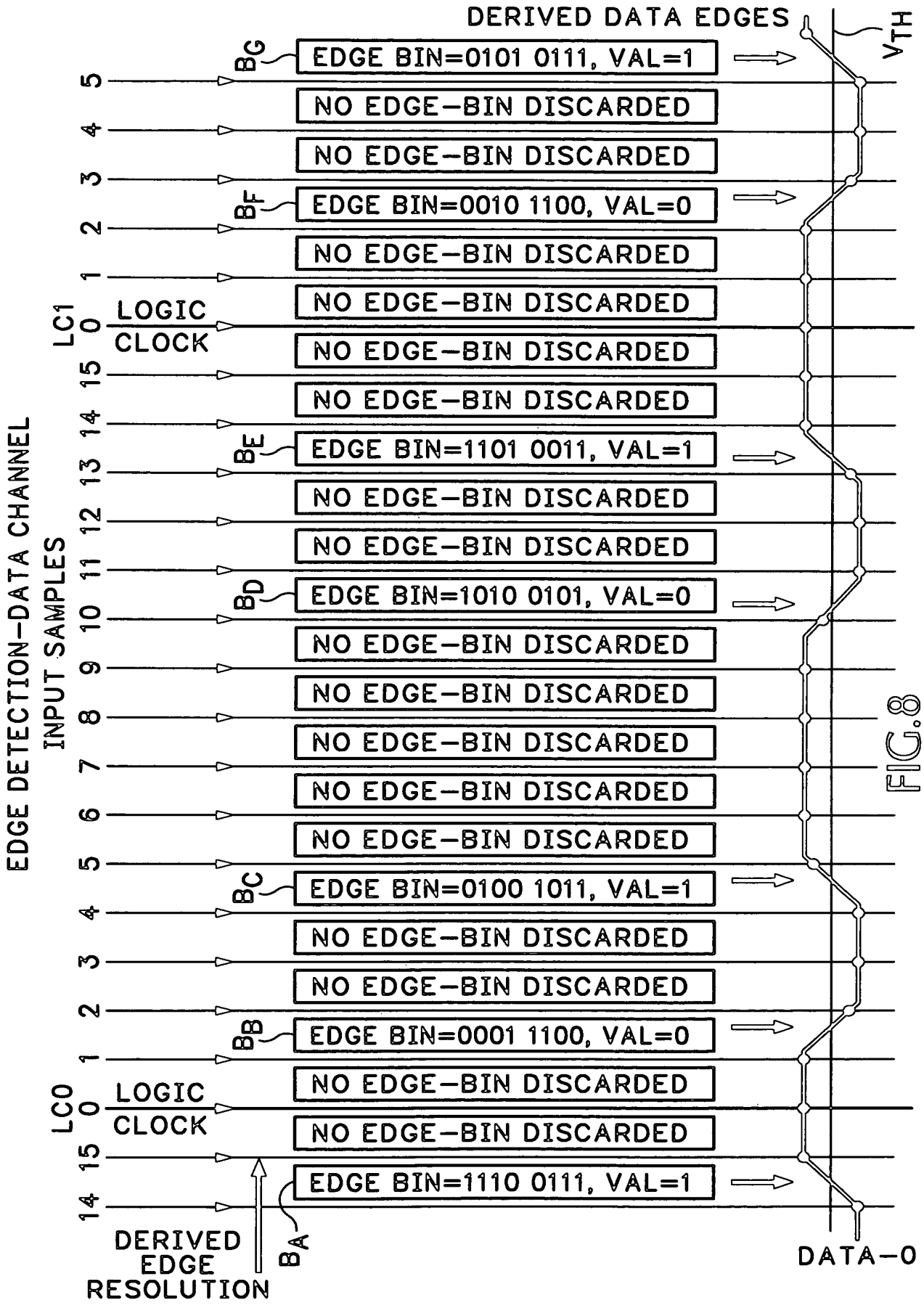
DERIVED DATA EDGES
V_{TH}
B_G
EDGE BIN=0101 0111, VAL=1
NO EDGE-BIN DISCARDED
NO EDGE-BIN DISCARDED
B_F
EDGE BIN=0010 1100, VAL=0
NO EDGE-BIN DISCARDED
NO EDGE-BIN DISCARDED
NO EDGE-BIN DISCARDED
B_E
EDGE BIN=1101 0011, VAL=1
NO EDGE-BIN DISCARDED
NO EDGE-BIN DISCARDED
B_D
EDGE BIN=1010 0101, VAL=0
NO EDGE-BIN DISCARDED
NO EDGE-BIN DISCARDED
NO EDGE-BIN DISCARDED
NO EDGE-BIN DISCARDED
NO EDGE-BIN DISCARDED
B_C
EDGE BIN=0100 1011, VAL=1
NO EDGE-BIN DISCARDED
NO EDGE-BIN DISCARDED
B_B
EDGE BIN=0001 1100, VAL=0
NO EDGE-BIN DISCARDED
NO EDGE-BIN DISCARDED
B_A
EDGE BIN=1110 0111, VAL=1
EDGE DETECTION-DATA CHANNEL
INPUT SAMPLES
LC1
LOGIC CLOCK
LC0
LOGIC CLOCK
DERIVED EDGE RESOLUTION
DATA-0
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

FIG.8

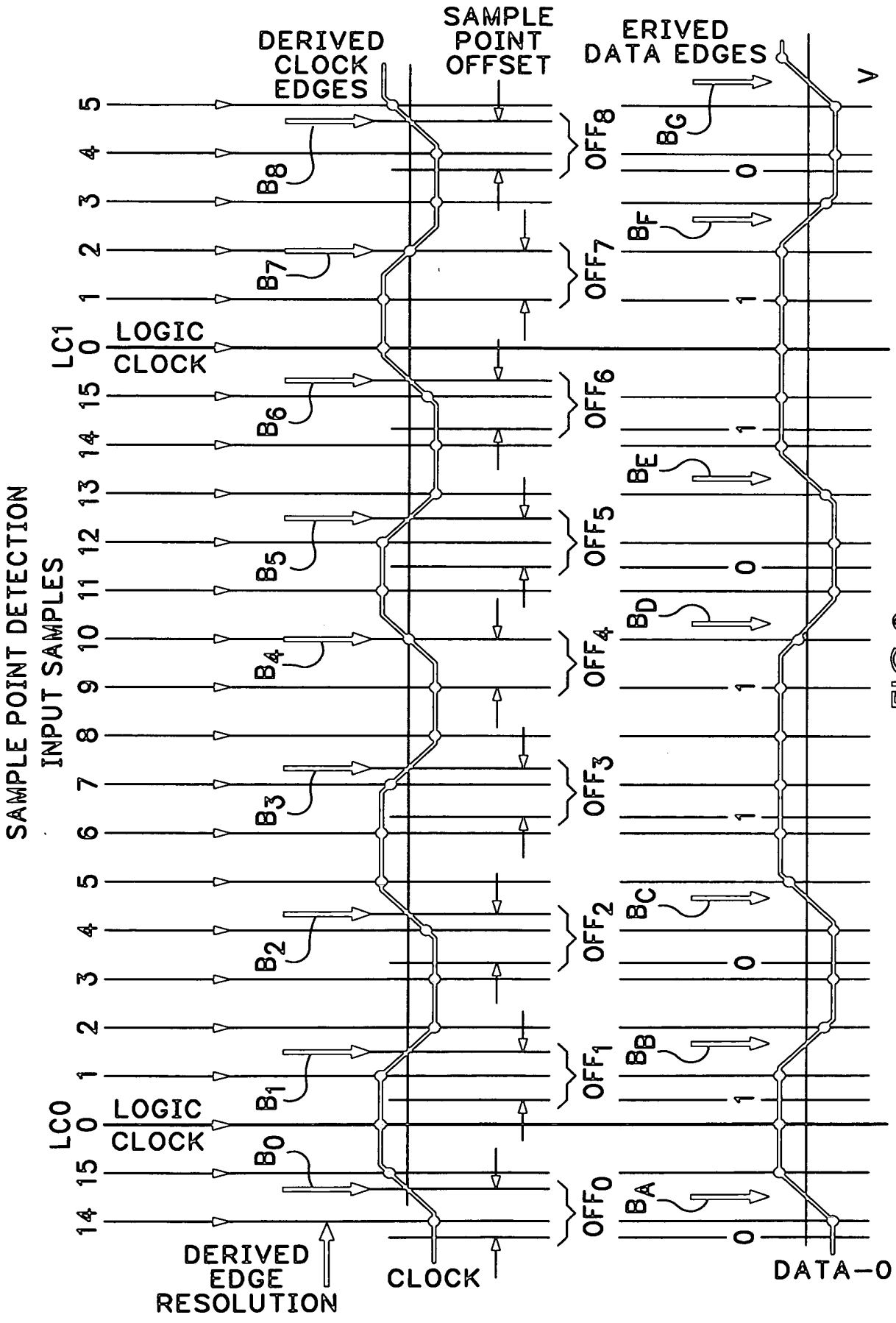
SAMPLE POINT DETECTION INPUT SAMPLES
DERIVED CLOCK EDGES
SAMPLE POINT OFFSET
ERIVED DATA EDGES
LC1
LOGIC CLOCK
LC0
LOGIC CLOCK
OFF8
OFF7
OFF6
OFF5
OFF4
OFF3
OFF2
OFF1
OFF0
B8
B7
B6
B5
B4
B3
B2
B1
B0
BG
BF
BE
BD
BC
BB
BA
DERIVED EDGE RESOLUTION
CLOCK
DATA-0

FIG.9

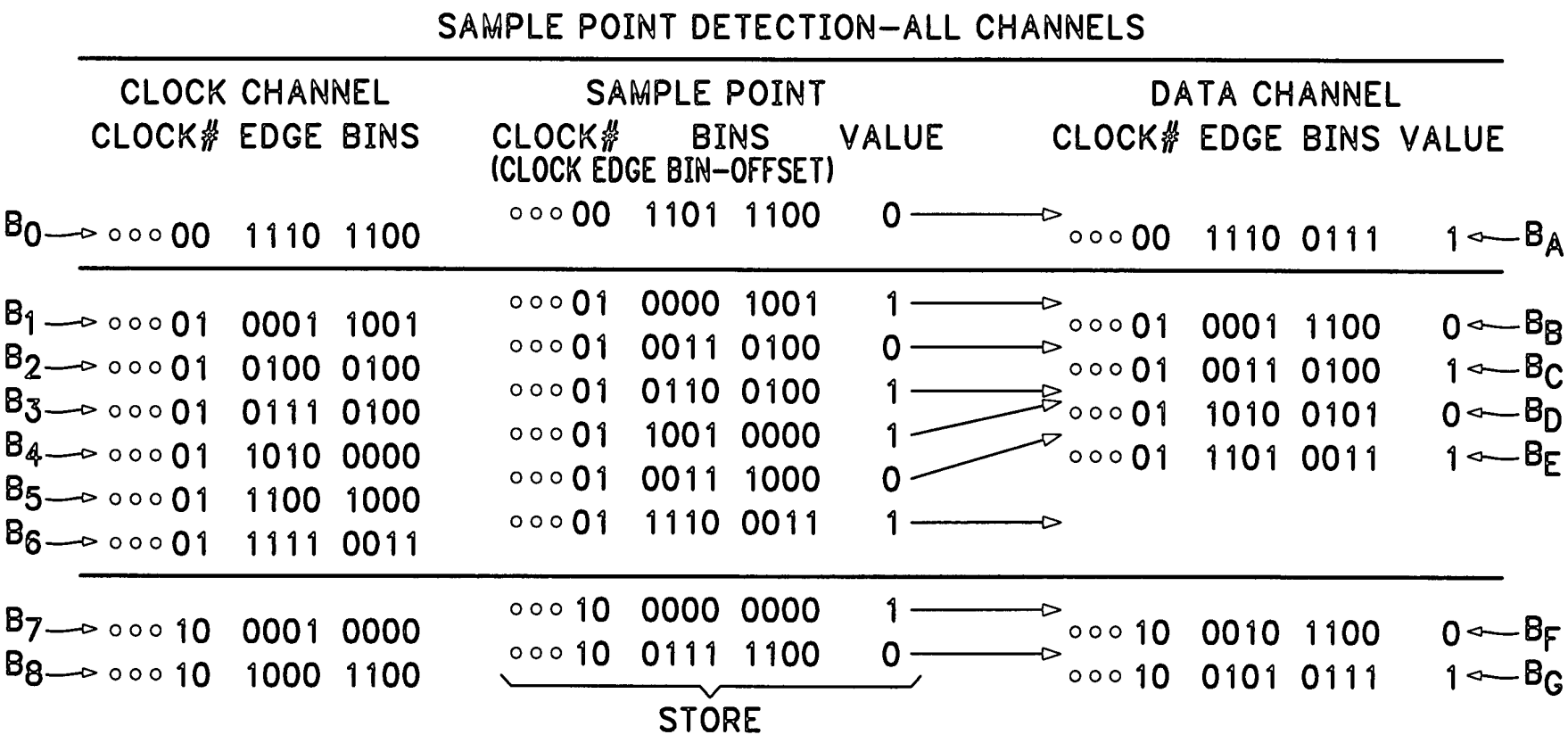
SAMPLE POINT DETECTION–ALL CHANNELS
CLOCK CHANNEL
CLOCK# EDGE BINS
SAMPLE POINT
CLOCK# BINS VALUE
(CLOCK EDGE BIN–OFFSET)
DATA CHANNEL
CLOCK# EDGE BINS VALUE
B0 ooo 00 1110 1100
ooo 00 1101 1100 0
ooo 00 1110 0111 1 B_A
B1 ooo 01 0001 1001
B2 ooo 01 0100 0100
B3 ooo 01 0111 0100
B4 ooo 01 1010 0000
B5 ooo 01 1100 1000
B6 ooo 01 1111 0011
ooo 01 0000 1001 1
ooo 01 0011 0100 0
ooo 01 0110 0100 1
ooo 01 1001 0000 1
ooo 01 0011 1000 0
ooo 01 1110 0011 1
ooo 01 0001 1100 0 B_B
ooo 01 0011 0100 1 B_C
ooo 01 1010 0101 0 B_D
ooo 01 1101 0011 1 B_E
B7 ooo 10 0001 0000
B8 ooo 10 1000 1100
ooo 10 0000 0000 1
ooo 10 0111 1100 0
ooo 10 0010 1100 0 B_F
ooo 10 0101 0111 1 B_G
STORE
SAMPLE POINT IS 100 ps BEFORE CLOCK EDGE
(SAMPLE POINT BIN = CLOCK EDGE BIN–0001 0000)

FIG.10